## REMARKS/ARGUMENTS

Favorable reconsideration and allowance of the present application are respectfully requested in view of the following remarks.

### A. SUMMARY OF THIS AMENDMENT

By the current amendment, Applicant:

1. Amends claim 1.
2. Respectfully traverses all prior art rejections.

This is in response to the Office Action dated November 7, 2008. Claims 1-6, 8, 10 and 11 are pending. Claims 1-6, 8, 10 and 11 stand rejected in the outstanding Office Action. Claim 1 has been amended.

### B. OBJECTION TO THE SPECIFICATION

The objection to the specification is respectfully traversed. The Examiner objected to the specification as allegedly not supporting the amendment filed July 9, 2008, that the partial contact between the second conductivity type layer and the front electrode is a straight line (the Examiner alleging that Figs. 1, 2, 5 and 6 show that the contact is a point and that Fig. 4 shows that the contact is a curvilinear line). Applicant submits that Figs. 5 and 6 clearly show that in one embodiment, the contact between the second conductivity type layer 65 (85) and the front electrode 68 (88) is a straight line (repeated periodically at the convex portions). The specification even explicitly states "The front electrodes 68 are formed linearly along the top of the convex portion, and *linearly* contact the N type semiconductor layer 65 at the top of the convex portions", p. 26, lines 7-9.

**C. PATENTABILITY OF THE CLAIMS**

The rejection of claim 11 under 35 U.S.C. § 112, first paragraph, as allegedly failing to comply with the written description requirement, is respectfully traversed. The Examiner stated that "Claim 11 requires the partial contact between the second conductivity type semiconductor layer and the front electrode to be a straight line, which is not disclosed in the specification". As discussed above, it is respectfully submitted that the specification clearly supports the limitations of claim 11 (e.g., that the partial contact is a straight line).

The rejection of claim 4 under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite, is respectfully traversed. More specifically, the Examiner stated that claim 4 (requiring the second conductivity type semiconductor layer becoming thicker as it goes from convex to concave portion of the substrate) is inconsistent with claim 1 from which it depends (requiring the second conductivity type semiconductor layer becoming thinner as it goes further from the contacted area).

Applicant submits that claim 4 is consistent with claim 1. Claim 1 requires that the second conductivity type semiconductor layer e.g., 85, becomes thinner as it *goes further from the contacted area*, e.g., 89 (see Fig. 6). Claim 4 requires that second conductivity type semiconductor layer e.g., 85, becomes thicker *from the top of the convex portions to the concave portions* of the substrate (see Fig. 6 again, where layer 85 is thinner at the top of the convex portions and becomes thicker as it goes towards the concave portions). Fig. 1 also represents claim 1. Claims 2 and 4 represent two different embodiments of the device of claim 1, wherein claim 2 is drawn to a device where the contacted area is at a *convex* region and claim 4 is drawn to a device where the contacted area is at a *concave* region.

The rejection of claims 1 and 8, as allegedly being anticipated under 35 U.S.C. § 102(b) by Nakai et al. (US 6,207,890) is respectfully traversed. Nakai fails to disclose or even remotely suggest each and every limitation set forth in the claims. Anticipation requires that "each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference", *Verdegaal Bro. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987) (MPEP § 2131).

Amended claim 1 now recites "a second conductivity type semiconductor layer formed on the surface of the first conductivity type semiconductor substrate and being in *direct* contact with said first conductivity type semiconductor substrate, *without any intervening layers therebetween*". Support for the amendment can be found, for example, in Fig. 1 of the instant specification. Nakai fails to teach or suggest this feature.

Nakai was cited in the previous Office Actions. Nakai fails to teach or suggest "the second conductivity type semiconductor layer being partially in contact with the front electrode", as required by claim 1. The Examiner identified layer 3 in Fig. 11 of Nakai as the claimed second type conductivity type semiconductor layer and layer 4 as the claimed front electrode. However, as can be clearly seen from Fig. 11, electrode 4 is in complete contact with layer 3. Nakai specifically states "A front electrode 4 is formed on the whole region of the p-type amorphous silicon layer 3", col. 1, lines 47-49.

In addition, amended claim 1 clearly distinguishes from Nakai, where layer 2 is disposed between n-type layer 1 and p-type layer 3. This rebuts Examiner's argument "(substrate 1 and layer 3) are indirectly contact each other, and therefore anticipates the instant claims", and "Examiner asserts that there is not a direct contact between convex portion of the substrate 1 and

electrode 4, however, they are indirectly contact each other, and therefore anticipates the instant claims", see section 11 on p. 8 of the Office Action.

Regarding claim 8, the Examiner referred to Fig. 6 of Nakai, and identified layer 1 as the claimed semiconductor substrate having convex and concave portions formed on its surface, and layer 2 as the claimed film containing second conductivity type impurities formed on the semiconductor substrate. However, Nakai does not teach or suggest (nor is it shown in Fig. 6) that layer 2 becomes thicker from the convex portion to the concave portion. Moreover, unlike the Examiner's assertion, the front electrode is layer 4 in Fig. 6 (see col. 11, lines 8-9 in Nakai), not layer 8 in Fig. 7, as stated by the Examiner, which layer 8 is a back electrode, see col. 11, lines 32-34 in Nakai. Front electrode 4 is not in partial contact with the concave portion. "indirect contact", as claimed by the Examiner, is not the same as "partial contact", required by the claim. Finally, by forming layer 2, which is an intrinsic amorphous silicon layer onto the substrate 1 does not imply that second type conductivity type impurities are implanted into the substrate 1. In the claimed device, this step corresponds to heating the N-type film formed on the substrate to diffuse the N-type impurities from the film to the substrate. This step is absent from Nakai.

The rejection of claim 6, as allegedly being anticipated under 35 U.S.C. § 102(b) by Nishitani et al. (US 6,023,020) is respectfully traversed.

Nishitani discloses a solar cell (Figs. 1-2) comprising a light absorbing layer 3 having convex and concave portions, a window layer 4 formed on the light absorbing layer 3, with a high-resistance thin film 6 formed between the light absorbing layer 3 and the window layer 4 (col. 1, lines 8-14, 41-42).

The Examiner identified the high-resistance thin film 6 as the claimed barrier film (e.g., serving as a barrier against impurity diffusion), and noted that film 6 becomes thicker from the convex portion to the concave portion (Figs. 1 and 2). Moreover, the Examiner identified window layer 4 as the means for implanting second conductivity type impurities into the semiconductor substrate 3 to form a second conductivity type semiconductor layer, and identified the transparent conductive film 5 as the claimed front electrode "that is in contact with the convex portion which constitutes a part of the semiconductor substrate surface (electrode 5 indirectly contacts the top surface of light absorbing layer".

Unlike the Examiner's assertion, front electrode 5 is not in partial contact with the convex portion which constitutes a part of the semiconductor substrate surface. First, conductive layer 5 is in complete contact with window layer 4 (see Figs. 1-2, and col. 3, lines 13-14 in Nishitani). Moreover, the claim language refers to "the convex portion which constitutes a part of the semiconductor substrate surface". The Examiner identified layer 3 as the claimed semiconductor substrate (see section 9(a) on p. 4 of the Office Action). However, electrode 5 is not even in contact with layer 3, as there are two intervening layers, 4 and 6 between the electrode 5 and the semiconductor substrate 3. Again, "indirect contact", as claimed by the Examiner, is not the same as "partial contact", required by the claim. Finally, by forming layer 4 onto the high-resistance film 6 does not imply that second type conductivity type impurities are implanted into the semiconductor substrate 3. In the claimed device, this step corresponds to heating the N-type film formed on the substrate to diffuse the N-type impurities from the film to the substrate. This step is absent from Nishitani.

For the above reasons, claims 1, 6 and 8 are allowable.

It is respectfully requested that the rejection of claims 2-5 and 10-11, all dependent from claim 1, also be withdrawn.

**D. MISCELLANEOUS**

In view of the foregoing and other considerations, all claims are deemed in condition for allowance. A formal indication of allowability is earnestly solicited.

The Commissioner is authorized to charge the undersigned's deposit account #14-1140 in whatever amount is necessary for entry of these papers and the continued pendency of the captioned application.

Should the Examiner feel that an interview with the undersigned would facilitate allowance of this application, the Examiner is encouraged to contact the undersigned.

Respectfully submitted,

**NIXON & VANDERHYE P.C.**

By: /Leonidas Boutsikaris/
Leonidas Boutsikaris
Reg. No. 61,377

LB:tlm
901 North Glebe Road, 11th Floor
Arlington, VA 22203-1808
Telephone: (703) 816-4000
Facsimile: (703) 816-4100